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EXAMINER

QUINTO, KEVIN V

ART UNIT

PAPER NUMBER

2826

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Please find below and/or attached an Office communication concerning this application or proceeding.

AR

Office Action Summary

Application No.

10/044,493

Applicant(s)

YU ET AL.

Examiner

Kevin Quinto

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 June 2003.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-10 and 20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-10 and 20 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ 6) ☐ Other: _____

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed June 12, 2003 have been fully considered but they are not persuasive.
2. In response to the arguments pertaining to the rejection of claims 1-4, 8, 9, and 20 under 35 U.S.C. 102(b) as being anticipated by Wilting, the examiner respectfully disagrees. Claim 1 contains the limitation "a gate dielectric from a high-K material" while the specification itself (p. 4, lines 18-24) defines a high-K material as a dielectric having a relative permittivity "of about ten (10) or more" and "of about twenty (20) or more." The examiner believes that the disclosed gate dielectric of Wilting, a combination of silicon oxide and silicon nitride, meets the limitation of the claim. The applicant has interpreted the combination of silicon oxide and silicon nitride to be silicon oxynitride (p. 7, Appeal Brief) which has a relative permittivity "of about 4-8." Given the breadth of the claim language, "made from a high-K material," and the language of the specification, "*of about* ten (10) or more," (emphasis added) the examiner believes that the relative permittivity of the silicon oxynitride gate dielectric qualifies as a high-K material.

3. The applicant has also filed arguments concerning the "source and drain consisting essentially of silicide" in claim 1 and the failure of Wilting to properly anticipate this limitation. The examiner addresses this limitation below in the section titled *Claim Rejections - 35 USC § 112*.

4. The examiner notes that the applicant disputes the rejection of claims 1-5, 8, 9, 10, and 20 under 35 U.S.C. 103(a) by citing the fabrication process that the applicant has disclosed. The examiner would like to note that:

Note that a "product by process" claim is directed to the product per se, no matter how actually made, *In re Hirao*, 190 USPQ 15 at 17 (footnote 3). See also *In re Thorpe*, 227 USPQ 964, 966; *In re Luck*, 177 USPQ 523; *In re Fessmann*, 180 USPQ 324; *In re Avery*, 186 USPQ 161; *In re Wertheim*, 191 USPQ 90 (209 USPQ 554 does not deal with this issue); and *In re Marosi et al.*, 218 USPQ 289, all of which make it clear that it is the patentability of the final product per se which must be determined in a "product by process" claim, and not the patentability of the process, and that an old or obvious product produced by a new method is not patentable as a product, **whether claimed in "product by process" claims or not**. Note that applicant has the burden of proof in such cases, as the above case law makes clear. See also MPEP 2113.

Therefore the examiner maintains the rejection of claims 1-5, 8, 9, 10, and 20 under 35 U.S.C. 103(a) because only the final product is relevant.

Claim Rejections - 35 USC § 112

5. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

6. Claims 1-10 and 20 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to

which it pertains, or with which it is most nearly connected, to make and/or use the invention.

7. Figure 1 of the current specification shows a source and a drain. The applicant maintains that the source and the drain are “essentially of silicide” in the claimed invention. The applicant cites the use of silicide for low parasitic resistance (p. 4, lines 1-4). The examiner would like to note that prior art silicon source and drain regions often have silicide contact layers *on their respective silicon surfaces* in order to attain low resistance contact regions (see USPN 4,657,628 or USPN 5,851,921). The silicon and the metal on top of it react to form the silicide. However figure 1 of the specification appears to show a source (20) and drain (22) which are completely made of silicide; there are no doped silicon regions which form the source or the drain. Doped silicon source and drain regions are necessary for a MOSFET; they provide the charge carriers (holes or electrons) which create the current flow. The specification makes no special note of the “essentially of silicide” source (20) and drain (22) regions or any doped silicon source or drain regions which are used in conjunction with these “essentially of silicide” source and drain regions. Because of this deficiency in the specification, the examiner has rejected claims 1-10 and 20 under 35 U.S.C. 112, first paragraph since figure 1 nor the specification discloses any doped silicon source and drain regions which allow the transistor to function. Due to the prior art knowledge of the uses of silicide and the lack of any figure in the specification showing doped silicon source and drain regions, the examiner has interpreted the limitation “source and drain consisting

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essentially of silicide" to mean a source and a drain region which have silicide contact regions. Wilting clearly follows this interpretation.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or
(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

9. Claims 1-4, 8, 9, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Wilting (USPN 4,080,719).

10. So far as understood in claims 1 and 2, Wilting (USPN 4,080,719) discloses a similar device. Figure 16 illustrates a MOSFET with a source (41) and a drain (42). Wilting discloses (column 7, lines 46-47) that the source (41) and drain (42) regions have silicide zones (31, 32). There is a semiconductor body disposed between the source (22) and the drain (23). There is a gate electrode (16A) disposed over the body; it is understood that the gate electrode (16A) defines a channel between the source (31) and the drain (32). There is a gate dielectric (4A, 4B), made of silicon oxide (4A) and silicon nitride (4B), which separates the gate electrode (16A) and the body. The silicon

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oxide – silicon nitride material is a well-known high-K or high dielectric film (see Lee, USPN 5,693,554, column 5, lines 30-31).

11. So far as understood in claims 3 and 4, Wilting discloses that the gate electrode (16A) is made of platinum silicide (column 6, lines 18-32) and can be made of other metal containing materials (column 7, lines 61-65).

12. So far as understood in claim 8, Wilting discloses the use of nickel silicide (column 7, lines 61-65) for the source and drain (31, 32). It is understood that the layer of semiconductor material, which is a part of the metal silicide, is a part of the body.

13. So far as understood in claim 9, figure 16 of Wilting shows that there is a liner (11) disposed adjacent or nearby sidewalls defined by the gate electrode (16A) and the gate dielectric (4A, 4B).

14. So far as understood in claim 20, figure 16 of Wilting shows that the silicide material of the source (31) and the semiconductor material of the body define a source/body junction. Figure 16 also shows that the silicide material of the drain (32) and the semiconductor material of the body define a drain/body junction.

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

16. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Wilting (USPN 4,080,719) in view of Venkatesan et al. (USPN 5,736,435).

17. So far as understood in claim 10, Wilting does not disclose the use of an SOI substrate (a semiconductor film disposed on an insulating layer, the layer being disposed on a semiconductor substrate). However the use of an SOI substrate is well known in the art. Venkatesan et al. (USPN 5,736,435, hereinafter referred to as the "Venkatesan" reference) discloses that SOI provides the advantages of reduced junction capacitance, large drive currents, high transconductance values, and immunity to short channel effects (column 1, lines 35-55). It would therefore be obvious to construct the device of Wilting on an SOI substrate so as to attain these benefits.

18. Claims 1-5, 8, 9, and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grant et al. (USPN 6,423,619 B1) in view of Wilting (USPN 4,080,719).

19. So far as understood in claims 1, 2, and 5, Grant et al. (USPN 6,423,619 B1, hereinafter referred to as the "Grant" reference) discloses a similar device. Figure 6 illustrates a MOSFET with a source (14) and a drain (16). There is a semiconductor body (12) disposed between the source (14) and the drain (16). There is a gate electrode (24, 26, 28) disposed over the body (12); it is understood that the gate electrode (24, 26, 28) defines a channel between the source (14) and the drain (16). There is a high-K gate dielectric (22), which can be made of hafnium oxide or zirconium oxide (column 2, lines 64-67), which separates the gate electrode (24, 26, 28) and the body (12). Grant does not disclose the use of source and drain regions with silicide

regions. However Wilting (USPN 4,080,719) discloses a device in figure 16 which utilizes source and drain regions with nickel silicide zones (column 7, lines 61-65). Furthermore Wilting discloses that silicides provide good conductivity; which is desirable in the semiconductor art (column 1, lines 22-40 and column 7, lines 46-60). It would therefore be obvious to utilize source and drain regions with silicide zones.

20. So far as understood in claims 3 and 4, Grant discloses that the gate electrode (25, 26, 28) can be made of a titanium nitride, tantalum nitride, tungsten, aluminum, ruthenium, and platinum (column 3, lines 1-5, 14-17, 30-33).

21. So far as understood in claims 8 and 20, Wilting discloses the use of nickel silicide (column 7, lines 61-65) for the source and drain (31, 32) which is a part of a layer of semiconductor material which makes up the body. The device of Grant constructed in view of Wilting has a source/body junction defined by the silicide material of the source and the semiconductor material of the body. The device of Grant constructed in view of Wilting also has a drain/body junction defined by the silicide material of the drain and the semiconductor material of the body. Figure 16 also shows that the silicide material of the drain (32) and the semiconductor material of the body define a drain/body junction.

22. So far as understood in claim 9, figure 6 of Grant shows that there is a liner (18) disposed adjacent or nearby sidewalls defined by the gate electrode (24) and the gate dielectric (22).

23. Claims 6 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Grant et al. (USPN 6,423,619 B1) in view of Wilting (USPN 4,080,719) as applied to

claim 1 above and further in view of Raajimakers et al. (United States Patent Application Publication No. US 2001/0031562 A1).

24. So far as understood in claims 6 and 7, Grant does not disclose the use of an oxide buffer layer. However it is well known in the art to provide an oxide buffer layer between a substrate and a high dielectric constant insulating film. Raajimakers discloses that a thin silicon oxide layer improves the interface between silicon and a high dielectric constant film (p.1, paragraph 7 and p.3, paragraph 33). It would therefore be obvious to use an oxide buffer layer in the device of Grant so as to attain this benefit. Grant and Raajimakers teach all of the claimed invention except for the exact thickness of the oxide layer. Although Grant and Raajimakers do not teach the exact oxide thickness as that claimed by Applicant:

The shape, size, dimension differences are considered obvious design choices and are not patentable unless unobvious or unexpected results are obtained from these changes. It appears that these changes produce no functional differences and therefore would have been obvious. Note In re Leshin, 125 USPQ 416.

Therefore claim 7 is not patentably distinguishable over the Grant and Raajimakers references.

14. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Grant et al. (USPN 6,423,619 B1) in view of Wilting (USPN 4,080,719) as applied to claim 1 above and further in view of Venkatesan et al. (USPN 5,736,435).

15. So far as understood in claim 10, neither Grant nor Wilting discloses the use of an SOI substrate (a semiconductor film disposed on an insulating layer, the layer being disposed on a semiconductor substrate). However the use of an SOI substrate is well known in the art. Venkatesan et al. (USPN 5,736,435, hereinafter referred to as the "Venkatesan" reference) discloses that SOI provides the advantages of reduced

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junction capacitance, large drive currents, high transconductance values, and immunity to short channel effects (column 1, lines 35-55). It would therefore be obvious to use an SOI substrate so as to attain these benefits in the device of Grant constructed in view of Wilting.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin Quinto whose telephone number is (703) 306-5688. The examiner can normally be reached on M-F 8AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (703) 308-6601. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7724 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

KVQ


Minhloan Tran
Primary Examiner
Art Unit 2826